AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-2 (canceled)

3. (currently amended) A semiconductor data processor comprising:

a first memory constituting a cache memory;

a second memory which can be used to provide a cacheable area or a non-cacheable area for the first memory; and

a read buffer which performs an operation to output data corresponding to a read access when the second memory is read accessed for the non-cacheable area,

wherein the read buffer temporarily holds predetermined access data and address data when the second memory is accessed for the non-cacheable area; and

~~The semiconductor data processor according to claim 2, wherein~~ the read buffer is connected to a first bus ~~at an~~ upstream therefrom in a transmission path ~~side~~ of a read request and is connected to a second bus ~~at a~~ downstream ~~side~~ therefrom in the transmission path of the read request,

and the second bus can transmit data in ~~the~~ a first number of parallel bits which is equal to or larger than ~~the~~ a second number of parallel access data bits [[by]] in the first bus.

4. (currently amended) The semiconductor data processor according to claim 3, wherein the read buffer ~~has~~ includes a data register ~~for holding~~ to hold read data to be transmitted ~~from the first memory~~ through the second bus, an address register ~~for holding~~ to hold an address of the data, and a control circuit ~~for causing~~ to cause the first bus to output the data of the data register for a read request of an address which is coincident with the address of the data held in the address register.

5. (currently amended) A semiconductor data processor comprising:

a first memory constituting a cache memory;

a second memory which can be used as a cacheable area or a non-cacheable area by the first memory; and

a read buffer which performs an operation to output data corresponding to a read access when the second memory is read accessed as the non-cacheable area,

wherein the read buffer temporarily holds predetermined access data and address data when the second memory is accessed as the non-cacheable area, and

~~The semiconductor data processor according to claim 1, wherein~~ the first bus and the second bus are dedicated sequential access buses.

6. (currently amended) The semiconductor data processor according to claim 5, further comprising a third bus ~~capable of connecting~~ which connects the first memory to the second memory in a ~~different~~ path different from a path formed by the first and second buses when the second memory is accessed [[as]] for the cacheable area.

7. (original) The semiconductor data processor according to claim 6, wherein a peripheral bus interface controller is connected to the third bus.

8. (original) The semiconductor data processor according to claim 6, further comprising an internal memory controller connected to the second bus and the third bus and serving to carry out an access interface control for the second memory.

9. (currently amended) The semiconductor data processor according to claim 8, wherein the third bus is provided with a secondary cache memory controller ~~for controlling~~ to control the second memory as a secondary cache memory for the first memory.

10. (currently amended) The semiconductor data processor according to claim 9, wherein the secondary cache memory controller ~~cache~~ invalidates the second memory in response to a signal indicative of a cache invalidation of the first memory.

11. (currently amended) The semiconductor data processor according to claim 9, further comprising a control register ~~for operably setting~~ which sets the internal memory controller and the secondary cache memory controller to operate exclusively of each other.

Claims 12-16 (canceled)

17. (currently amended) ~~The~~ A semiconductor data processor ~~according to claim 16, further~~ comprising:

a first memory constituting a cache memory;

a second memory which can be used to provide a secondary cache memory or memory which is not cache memory for the first memory;

a designator which selectively designates an area of the second memory as secondary cache memory or memory which is not cache memory;

a secondary cache memory controller which performs an access interface control to the second memory area as secondary cache memory;

an internal memory controller which performs access interface control to the second memory area as memory which is not cache memory; and

a read buffer ~~capable of carrying out~~ which performs an operation ~~for outputting~~ to output data, ~~corresponding to a read access~~ read from the second memory area via the internal memory controller, when the second memory area is read accessed as ~~the non-cacheable area~~ memory which is not cache memory by the internal memory controller.

18. (currently amended) The semiconductor data processor according to claim 17, wherein the read buffer newly holds data and an address corresponding to an access if it does not retain data corresponding to the access when the second memory area is accessed as ~~the non-cacheable area~~

memory which is not cache memory by the internal memory controller.

19. (currently amended) The semiconductor data processor according to claim 18, wherein the read buffer is connected to a first bus ~~at an~~ upstream therefrom in a transmission path ~~side~~ of a read request and is connected to a second bus, having a greater bus width than a width of the first bus, ~~at a~~ downstream therefrom in the transmission path ~~side~~ of the read request.